December 5th-6th, 2018 | San Jose, CA

Applying SIMD Optimizations to DPCLS

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OVERVIEW

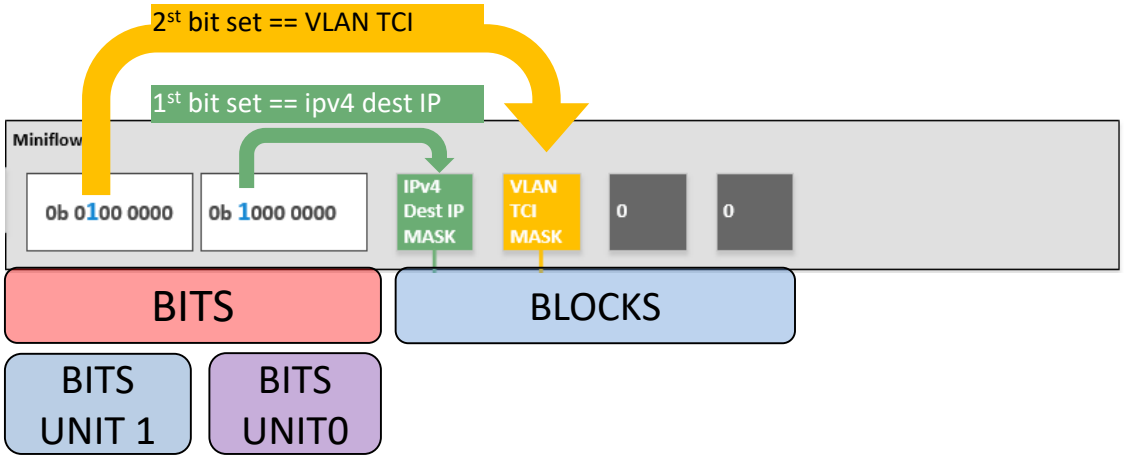
- Introduction
  - Vectorization
  - Miniflow
  - Datapath Classifier
- AVX-512 DPCLS
  - Graphical Walkthrough
- Future Work

VECTORIZATION

- **More work per CPU cycle**
- SIMD : **S**ingle **I**nstruction **M**ultiple **D**ata
- AVX-512
  - 512-bit wide registers
  - “Lanes” concept
    - 512 bits split
    - 8 lanes x 64 bits
    - A lane is a packet

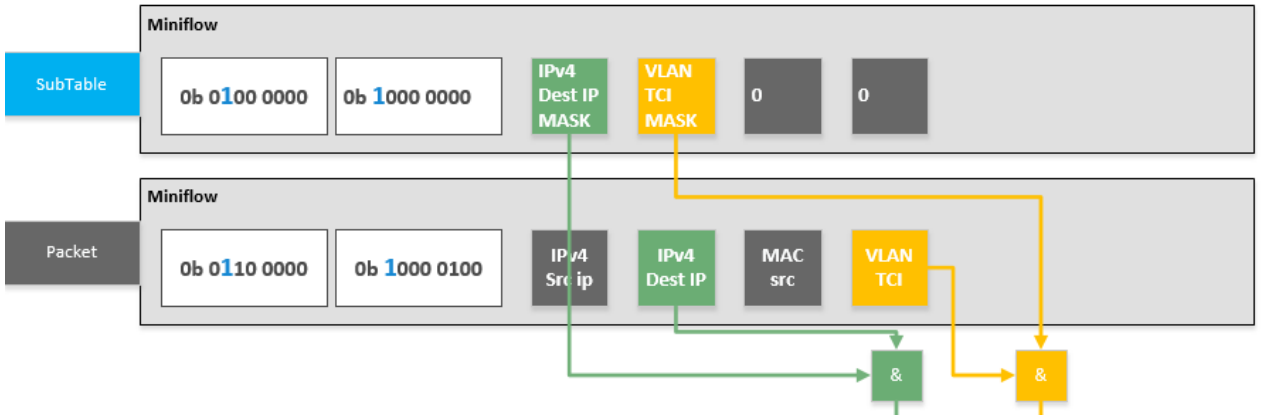
MINIFLOW

- **What is a miniflow?**
  - Structure to represent metadata
  - Packets and Subtables have miniflows

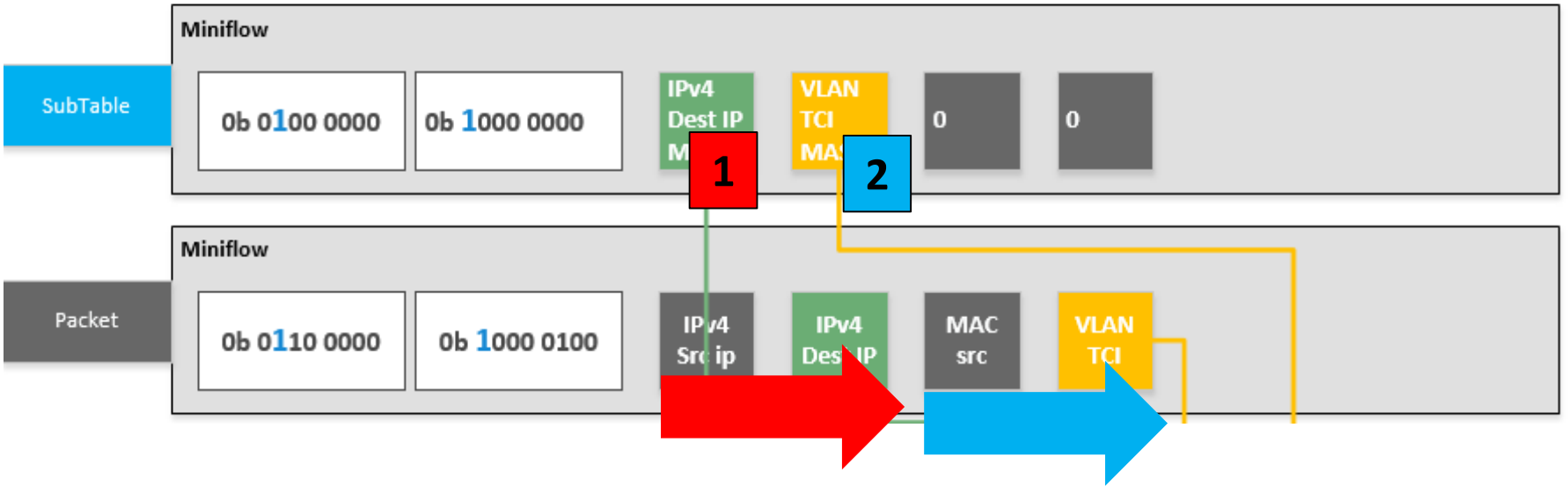


DATA PATH CLASSIFER

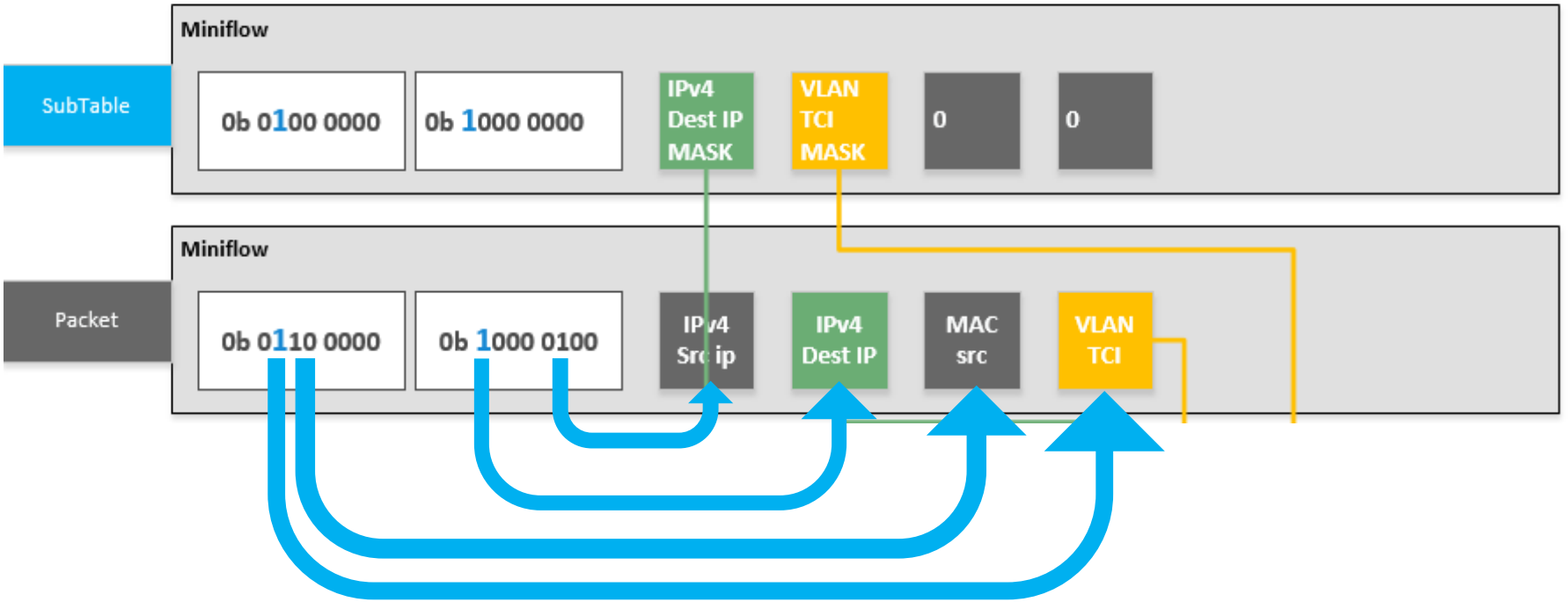
- Iterate Subtable BITS
  - Find Corresponding Packet Block, Mask with Subtable



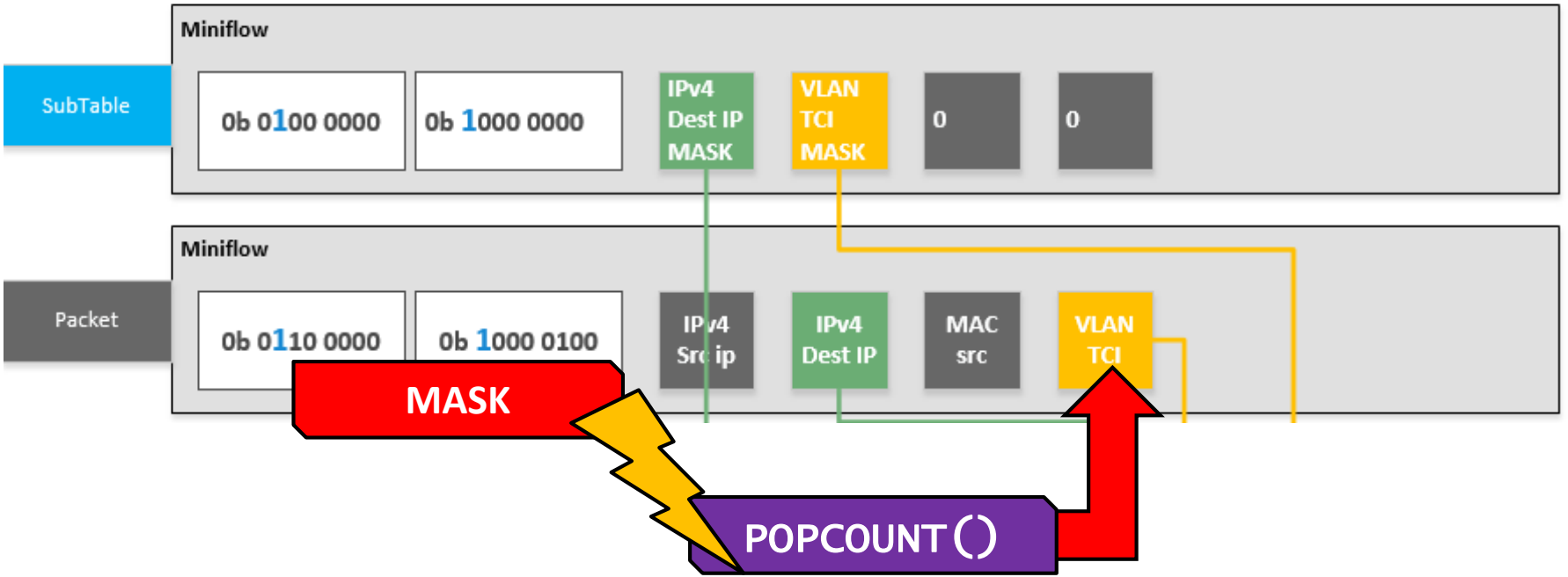
CURRENT CODE



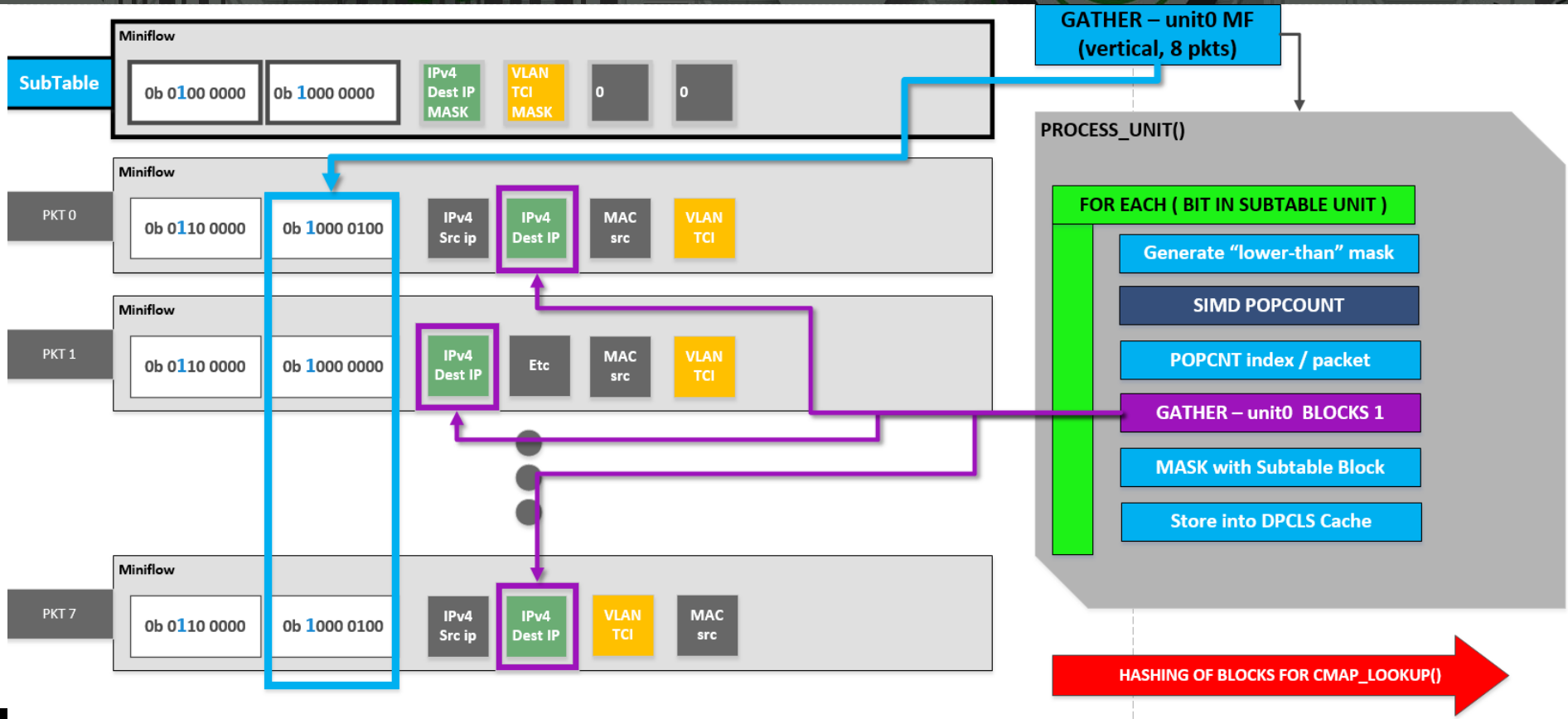
BITS-TO-BLOCKS



POPCOUNT()


Miniflow
SubTable
0b 0100 0000
0b 1000 0000
IPv4 Dest IP MASK
VLAN TCI MASK
0
0
Miniflow
Packet
0b 0110 0000
0b 1000 0100
IPv4 Src ip
IPv4 Dest IP
MAC src
VLAN TCI
MASK
POPCOUNT ()

POPCOUNT() + AVX-512



FUTURE WORK

- **Per-Subtable Function pointers**
  - Flexible selection of Optimized Functions
  - Using Context of Subtable Miniflow
    - Benefits scalar code too!

- **Optimize Cache Utilization**
  - EMC – Fast / Cache trashes > X flows
  - SMC – Fast / More Efficient cache usage
  - DPCLS – Slow(er) / Consistent w flow-count

CALL TO ACTION

- **Community to Drive SW Optimizations**
  - **Require well defined use-cases to optimize**
  - **Request to community to contribute use-cases**

- **Tuning Knobs**
  - **OVS community : “Less is More”**
  - **Suggestion : “Use CPU to go faster” button?**
    - **Enables AVX in DPCLS**
    - **Other CPU specific opts?**

? Questions ?

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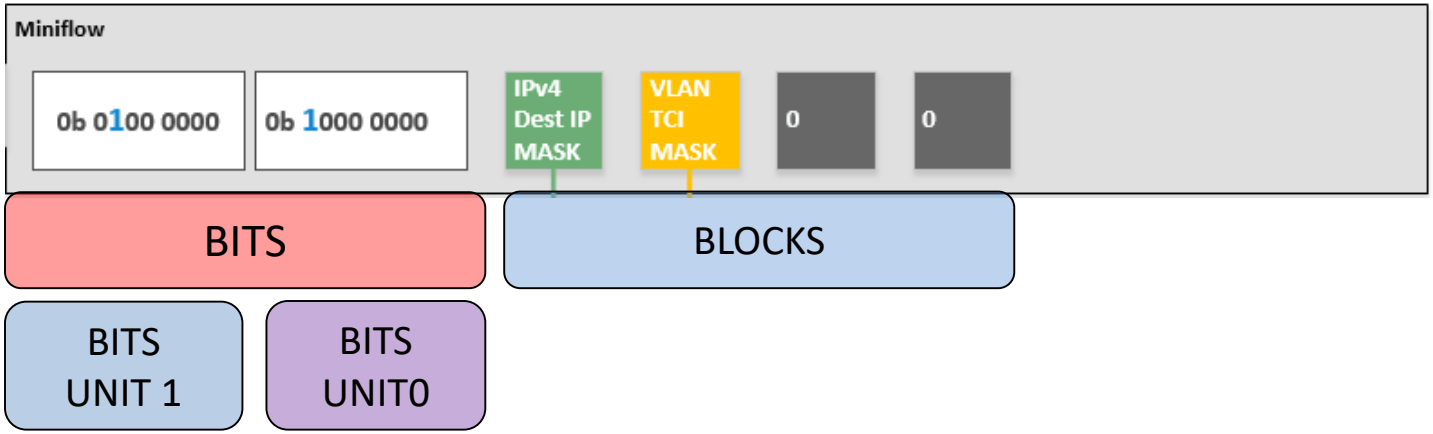
Patchwork series 77134 : “dpcls subtable miniflow optimizations”

MINIFLOW

MINIFLOW LEDGEND:



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