



↔ vs

Open vSwitch

December 10th-11th, 2019 | Westford, MA

**Next Steps for Software Datapath**

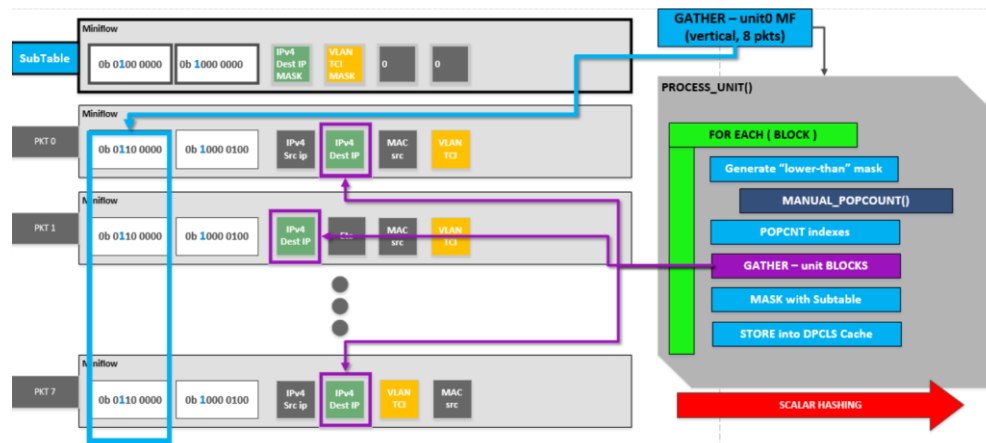
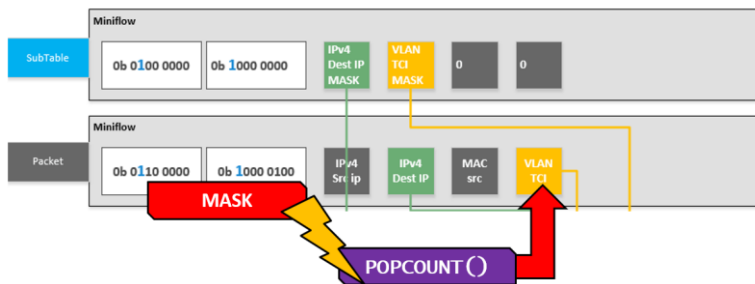
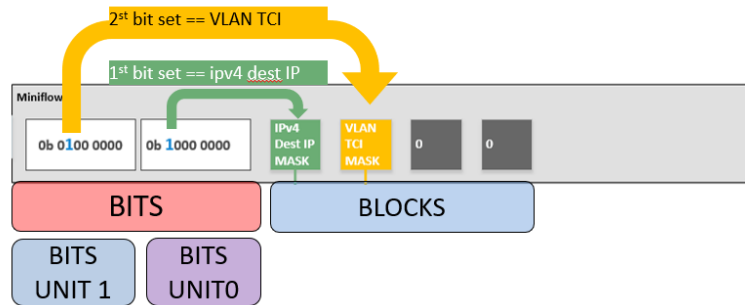
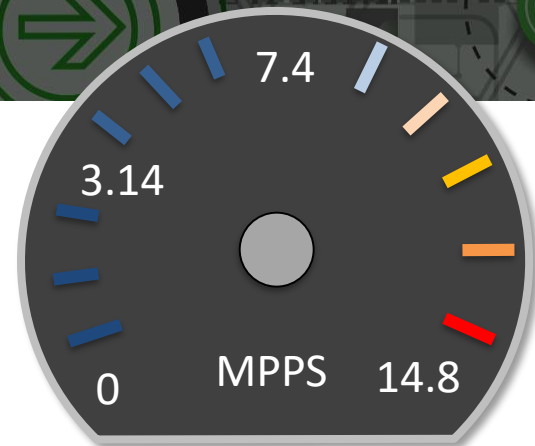
Harry van Haaren  
Intel

# Introduction

- **GOOD** is Higher Performance
- **GREAT** is “Batteries-Included” Experience

# Performance

- The “SIMD DPCLS” talk at OVS ‘18

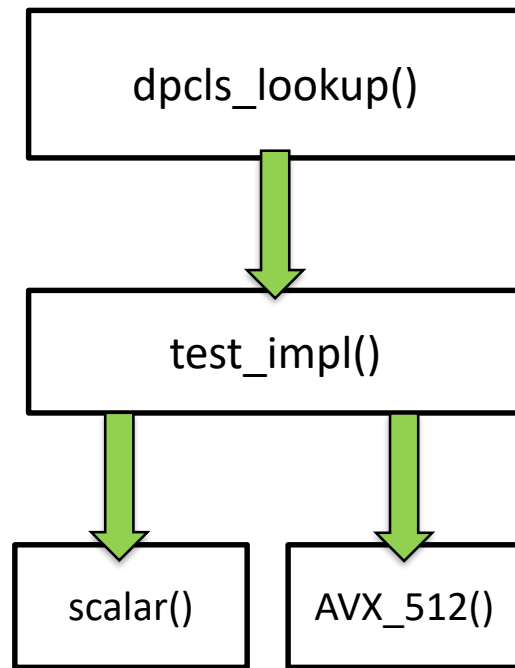


# Batteries Included

- **Test & Validation**
  - Minimal Extra Effort per Release
  - Smart Automated Testing
- **Usability & Debug**
  - Users to Check Status
  - Power-Users to Configure
- **Packaged & Deploy**
  - Transparent Acceleration

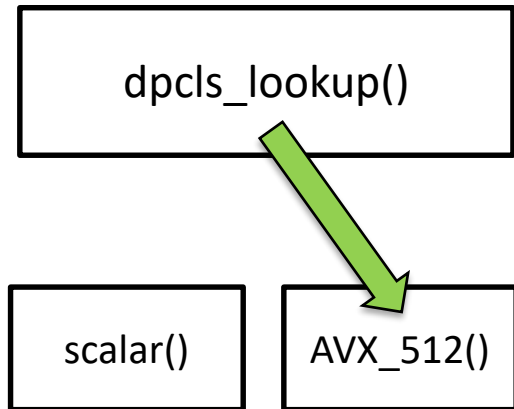
# Test & Validation

- **ISA Optimized DPCLS**
  - Scalar
  - AVX-512
- **Automated Testing**
  - DPCLS Function Pointer re-use
  - “Delegator” implementation
  - Tests all other implementations
  - Validates results as Identical
  - Runs with all Unit Tests

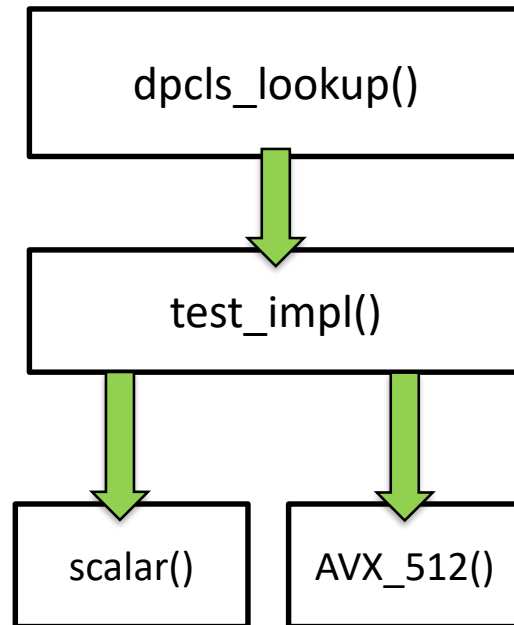


# Test & Validation

## DEPLOYED



## TESTING

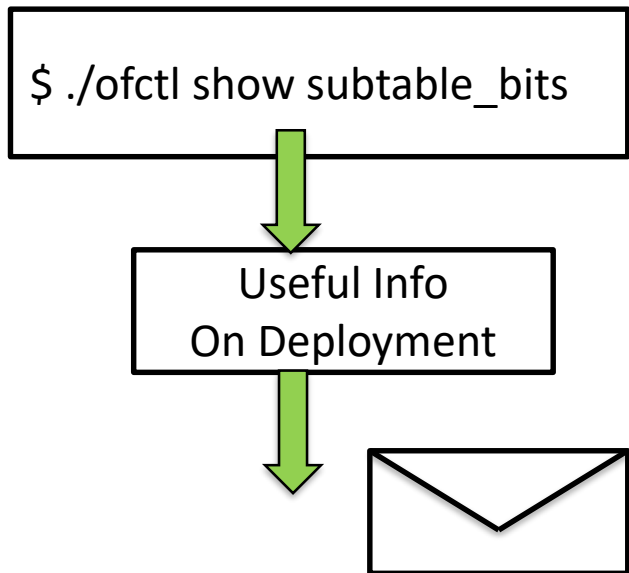


# Usability & Debug

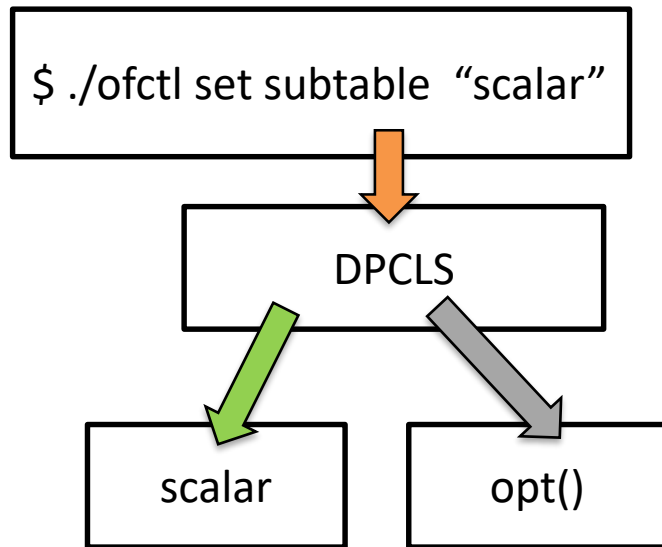
- **Easily View Status**
  - Understand Optimizations that are in use
  - Provide Feedback to OVS Community
- **Enable Power-Users to Configure**
  - Reset Optimized Version to Scalar
  - Sometime, Somebody will want this
    - Exact replication of a deployment?

# Usability & Debug

## User



## Power User



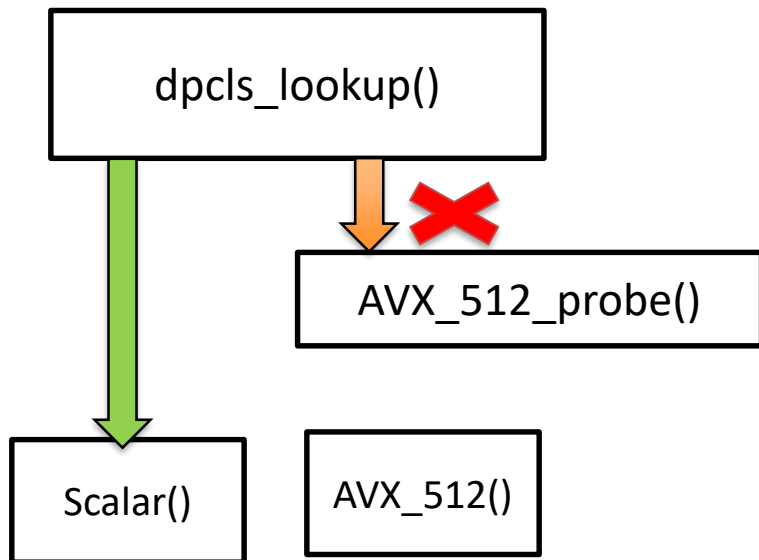


# Package & Deploy

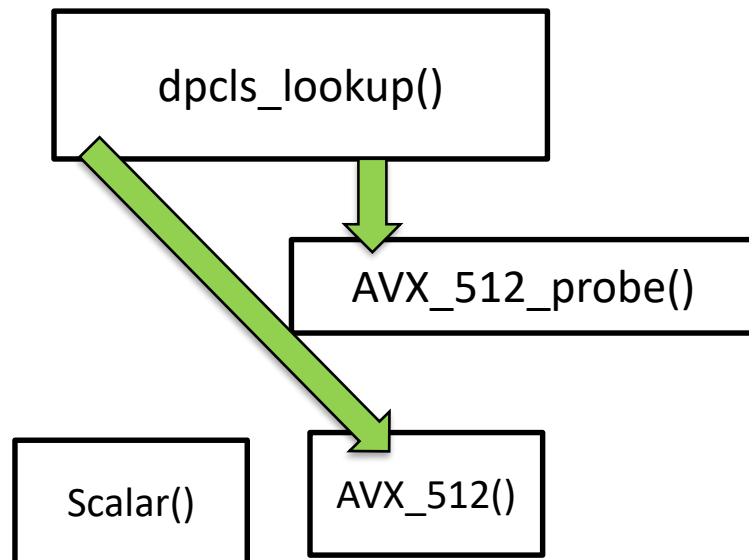
- **Runtime CPU Detection**
  - Required to “plug in” ISA-based optimizations
- **RFC/Patch v1 on mailing list soon**
  - Based on DPDK EAL CPU Detection
- **One Binary Runs Everywhere**
  - Build process updates

# Runtime CPU Detection

## CPU without ISA

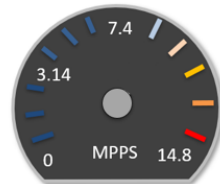


## CPU with ISA

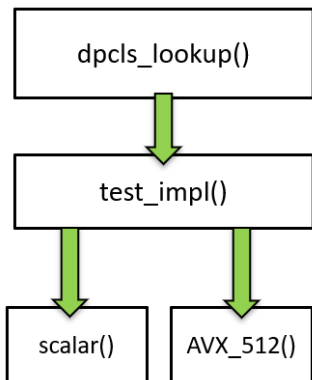


# Summary

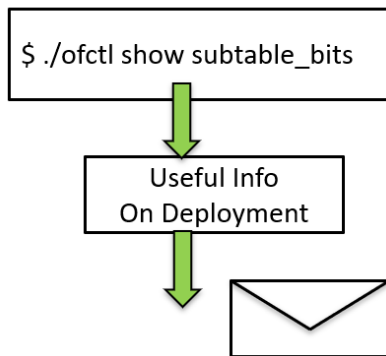
## PERFORMANCE OPTIMATIONS



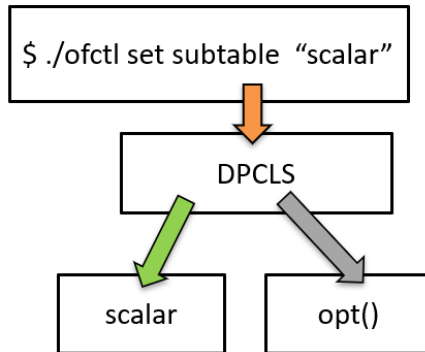
### Validation



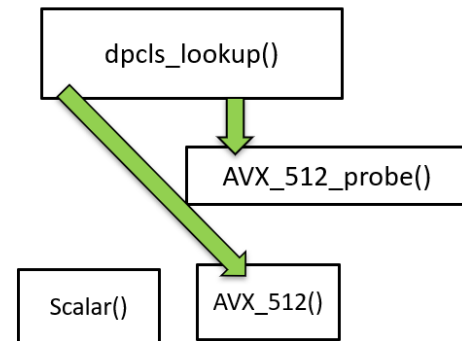
### Usability



### Easy Debug



### Packaged





**! Thanks !**  
**? Questions ?**

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