Applying SIMD Optimizations to DPCLS

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OVERVIEW

• Introduction
  – Vectorization
  – Miniflow
  – Datapath Classifier

• AVX-512 DPCLS
  – Graphical Walkthrough

• Future Work
VECTORIZATION

- More work per CPU cycle
- SIMD: **Single Instruction Multiple Data**
- AVX-512
  - 512-bit wide registers
  - “Lanes” concept
    - 512 bits split
    - 8 lanes x 64 bits
    - A lane is a packet
• **What is a miniflow?**
  • Structure to represent metadata
  • Packets and Subtables have miniflows
• Iterate Subtable BITS
  • Find Corresponding Packet Block, Mask with Subtable
POPCOUNT() + AVX-512

GATHER – unit0 MF (vertical, 8 pkts)

FOR EACH (BIT IN SUBTABLE UNIT)
- Generate “lower-than” mask
- SIMD POPCOUNT
- POPCNT index / packet
- GATHER – unit0 BLOCKS 1
- MASK with Subtable Block
- Store into DPCLS Cache

HASHING OF BLOCKS FOR CMAP_LOOKUP()
FUTURE WORK

• Per-Subtable Function pointers
  • Flexible selection of Optimized Functions
  • Using Context of Subtable Miniflow
    • Benefits scalar code too!

• Optimize Cache Utilization
  • EMC – Fast / Cache trashes > X flows
  • SMC – Fast / More Efficient cache usage
  • DPCLS – Slow(er) / Consistent w flow-count
CALL TO ACTION

• Community to Drive SW Optimizations
  • Require well defined use-cases to optimize
  • Request to community to contribute use-cases

• Tuning Knobs
  • OVS community : “Less is More”
  • Suggestion : “Use CPU to go faster” button?
    • Enables AVX in DPCLS
    • Other CPU specific opts?
? Questions ?

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Patchwork series 77134 : “dpcls subtable miniflow optimizations”
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